Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus for driving a CCD image sensor which performs charge transfer operation in accordance with a pulse signal, comprising:

a drive circuit for supplying a pulse signal to the CCD image sensor; and

a power supply circuit, connected to the drive circuit, for supplying the drive circuit with a voltage for generating the pulse signal, wherein the power supply circuit includes an over-boosting circuit for temporarily over-boosting the voltage supplied to the drive circuit to generate an over-boosted voltage exceeding a target control voltage for a predetermined time, prior to the charge transfer operation of the CCD image sensor.

2. (Original) The apparatus according to claim 1, wherein the

power supply circuit includes a constant voltage control circuit that performs constant voltage control on the voltage supplied to the drive circuit, and wherein the constant voltage control circuit is inactivated when the over-boosting circuit is executing an over-boosting operation.

3. (Original) The apparatus according to claim 2, wherein the over-boosting circuit is a charge pump type boosting circuit that performs a boosting operation in accordance with a clock signal, and the constant voltage control circuit thins the clock signal in the constant voltage control and supplies a thinned clock signal to the charge pump type boosting circuit, and wherein constant voltage control circuit supplies the clock signal without thinning the clock signal to the charge pump type boosting circuit when the charge pump type boosting circuit performs the over-boosting operation.

4. (Original) The apparatus according to claim 1, wherein the CCD image sensor is a frame transfer type CCD image sensor including an image sensing section for generating charges by performing photoelectric conversion and a storage section, located separate from the image sensing section, for temporarily storing charges transferred from the image sensing section; and wherein the drive circuit includes a vertical driver for generating a pulse signal for charge transfer from the image sensing section to the storage section.

5. (Original) The apparatus according to claim 1, wherein the drive circuit and the power supply circuit are formed on a single semiconductor integrated circuit substrate.

6. (Original) The apparatus according to claim 5, wherein the CCD image sensor generates an image sensor output signal in accordance with charges every predetermined period, and the power supply circuit is enabled when the CCD image sensor is stopping generation of the image sensor output signal.

7. (Currently Amended) An apparatus for driving a CCD image sensor which performs charge transfer operation in accordance with a pulse signal, comprising:

a drive circuit for supplying a pulse signal to the CCD image sensor, and

a power supply circuit, connected to the drive circuit, for supplying the drive circuit with a voltage for generating the pulse signal; and wherein the drive circuit and the power supply circuit are formed on a single semiconductor integrated circuit substrate, wherein the CCD image sensor generates an image sensor output signal every predetermined period in accordance with charges, and the power supply circuit is enabled when the image sensor stops generating image sensor output signals.

8. Cancelled.

9. (Original) The apparatus according to claim 7, wherein the CCD image sensor is a frame transfer type CCD image sensor including an image sensing section for generating charges by performing photoelectric conversion and a storage section, located separate from the image sensing section, for temporarily storing charges transferred from the image sensing section, and wherein the drive circuit includes a vertical driver for generating a pulse signal for charge transfer from the image sensing section to the storage section.

10. (Original) The apparatus according to claim 7, wherein the power supply circuit includes a charge pump type boosting circuit for performing a boosting operation in accordance with a clock signal.

11. (Original) The apparatus according to claim 10, wherein the power supply circuit includes a constant voltage control circuit for thinning a clock signal and supplying a thinned clock signal to the charge pump type boosting circuit to perform constant voltage control on the voltage supplied to the drive circuit, the constant voltage control circuit supplies the clock signal without thinning to the charge pump type boosting circuit prior to the charge transfer operation of the CCD image sensor, and wherein the charge pump type boosting circuit temporarily over-boosts the voltage supplied to the drive circuit from the power supply circuit in accordance with the clock signal to produce an over-boosted voltage.

12. (Withdrawn) A buffer circuit comprising:

a CMOS inverter circuit including a P channel MOS transistor and an N channel MOS transistor, which are connected in series, an input signal being supplied to gates of the P channel and N channel MOS transistors; and

a timing adjusting circuit, connected to the CMOS inverter circuit, for adjusting a timing of supplying the input signal to the gates of the P channel and N channel MOS transistors such that the P channel and N channel MOS transistors are turned on at different timings.

13. (Withdrawn) The buffer according to claim 12, wherein the timing adjusting circuit includes a logic circuit for supplying first and second switching signals to the gates of the P channel and N channel MOS transistors such that in a period during which one of the P channel and N channel MOS transistors is turned off, the other one of the P channel and N channel MOS transistors is turned on.

14. (Withdrawn) The buffer according to claim 12, wherein the timing adjusting circuit includes:

an OR circuit having a first OR input terminal for receiving the input signal, a second OR input terminal, and an OR output terminal connected to the gate of the P channel MOS transistor; and

an AND circuit having a first AND input terminal for receiving the input signal, a second AND input terminal connected to the OR output terminal of the OR circuit, and an AND output terminal connected to the gate of the N channel MOS transistor.

15. (Withdrawn) The buffer according to claim 12, wherein the timing adjusting circuit includes:

a first delay circuit for supplying a first delayed input signal to the gate of the P channel MOS transistor such that an ON timing of the P channel MOS transistor is delayed and an ON duration of the P channel MOS transistor is shorter than an OFF duration of the N channel MOS transistor; and

a second delay circuit for supplying a second delayed input signal to the gate of the N channel MOS transistor such that an ON timing of the N channel MOS transistor is delayed and an ON duration of the N channel MOS transistor 10 is shorter than an OFF duration of the P channel MOS transistor.

16. (Withdrawn) The buffer according to claim 15, wherein a signal falling time constant of the first delay circuit at a time of signal inversion is greater than a signal falling time

constant of the second delay circuit, and a signal rising time constant of the second delay circuit is greater than a signal rising time constant of the first delay circuit.

17. (Withdrawn) A driver comprising:

a plurality of functional circuits including a first functional circuit having a relatively high frequency of operations and a second functional circuit having a relatively low frequency of operations, the first functional circuit including a first buffer circuit having a first CMOS inverter circuit having a first P channel MOS transistor and a first N channel MOS transistor, which are connected in series, and

a first timing adjusting circuit, connected to the first CMOS inverter circuit, for supplying first and second switching signals to gates of the first P channel MOS transistor and the first N channel MOS transistor such that in a period during which one of the first P channel and first N channel MOS transistors is turned off, the other one of the first P channel and first N channel MOS transistors is turned on, the second functional circuit including a second buffer circuit having a second CMOS inverter circuit having a second P channel MOS transistor and a second N channel MOS transistor, which are connected in series, and

a second timing adjusting circuit, connected to the second CMOS inverter circuit, for receiving an input signal and supplying a third switching signal to the gate of the second P channel MOS transistor such that an ON timing of the second P channel MOS transistor is delayed and an ON duration of the second P channel MOS transistor is shorter than an OFF duration of the second N channel MOS transistor, wherein second timing adjusting circuit supplies a fourth switching signal to the gate of the second N channel MOS transistor such that an ON timing of the second N channel MOS transistor is delayed and an ON duration of the second N channel MOS transistor is shorter than an OFF duration of the second P channel MOS transistor.

18. (Withdrawn) The driver according to claim 17, wherein the first timing adjusting circuit includes:

an OR circuit having a first OR input terminal for receiving the input signal, a second OR input terminal, and an OR output terminal connected to the gate of the P channel MOS transistor, and an AND circuit having a first AND input terminal for receiving the input signal; a second AND input terminal, which connected to the OR output terminal of the OR circuit, and an AND output terminal connected to the gate of the N channel MOS transistor; and

the second timing adjusting circuit includes:

a first inverter circuit for generating the third switching signal, and

a second inverter circuit for generating the fourth switching signal, wherein a signal falling time constant of the first inverter circuit at a time of signal inversion is greater than a signal falling time constant of the second inverter circuit while a signal rising time constant of the second inverter circuit is greater than a signal rising time constant of the first inverter circuit.

19. (Withdrawn) The driver according to claim 17, wherein the driver drives a CCD image sensor; the first functional circuit is a first charge pump which includes at least one first pumping capacitor and generates a boosted voltage by using the first pumping capacitor, and the first buffer circuit of the first charge pump buffers a first pumping clock signal and supplies the buffered first pumping clock signal to the first pumping capacitor; and

the second functional circuit is one of a pulse-signal generating circuit and a second charge pump, the pulse signal generating circuit receives the boosted voltage from the first charge pump and generates a pulse signal used in the charge transfer operation of the CCD image sensor, the second buffer circuit of the pulse-signal generating circuit is used as a pulse-signal output buffer circuit, and wherein the second charge pump includes at least one second pumping capacitor and generates a bias voltage supplied to the CCD image sensor, and the second buffer circuit of the second charge pump buffers a second pumping clock signal and supplies the buffered second pumping clock signal to the second pumping capacitor.